A SINGLE CHIP X-BAND PHASE SHIFTER WITH 6 BIT UNCORRECTED PHASE RESOLUTION AND MORE THAN 8 BIT CORRECTED PHASE RESOLUTION

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ABSTRACT

The design, fabrication, performance and production results of a GaAs monolithic phase shifter, based on a vector modulator principle, are described. The device exhibits a typical RMS phase error of about 3 degrees and an RMS amplitude error less than 0.30 dB across the frequency band from 7.0 - 10.5 GHz and over a linear controllable gain range of 15 dB. Typical insertion gain is 0 dB, input return losses are better than 15 dB and output return losses are better than 10 dB. The device is intended for application in a wide-band active phased-array antenna.
The analogue control of the device enables the correction of the systematic phase errors and amplitude errors. Tests have demonstrated that through phase correction the RMS phase error is reduced to less than 0.7 degrees while the RMS amplitude error is still less than 0.30 dB.

INTRODUCTION

The main requirements of GaAs MMIC circuits for application in transmit/receive modules of phased-array antennas are: high performance, high yield, short test time cycles and low handling and mounting costs.
Next-generation multifunction phased-array radars will operate at X-band and exhibit a 30% to 40% bandwidth. These radars will be equipped with features like phase-only nulling or main-lobe nulling. In addition, the low sidelobe demands put stringent requirements on the amplitude and phase accuracy of the applied transmit/receive modules. Thus, 6 or 7 bit phase shifters which exhibit also a small RMS amplitude error are required.
Recent publications dealt with 6-bit digital phase shifters, [2], or low-cost 5-bit analogue phase shifters at X-band [1]. These reported phase shifters do not meet the phase and amplitude requirements mentioned. In addition reported insertion losses and noise figures tend to be too high.
In this paper a GaAs MMIC single-chip analogue phase shifter is presented which achieves a typical RMS phase error of 3 degrees while the associated RMS amplitude error is less than 0.3 dB. This phase error is maintained over an independent controllable gain range of 15 dB.
In addition, correction of the systematic phase errors leads to an RMS phase error in the range from 0.28 to 0.7 degrees and an RMS amplitude error less than 0.30 dB respectively.
The results are verified with a large number on-wafer measurements. The device is successfully implemented in a phased-array TR module demonstrator.

PHASE SHIFTER DESIGN

The phase-shifter design is based on a vector modulator, [3]. A simplified block diagram is shown in figure 1. The active quadrature power splitter consists of a 2-stage feedback amplifier with flat gain and relative low-noise behaviour. The quadrature phase relationship is obtained by lumped element high-pass and low-pass filters. Each filter is cascaded with an active isolator in order to ensure the quadrature phase relationship under different bias, load and temperature conditions. The biphase modulators consist of a two-stage differential amplifier and a double-balanced FET mixer. The double balanced structure is chosen to guarantee the extreme required degree of linearity. Finally, the outputs of the biphase modulators are summed by an active in-phase combiner.

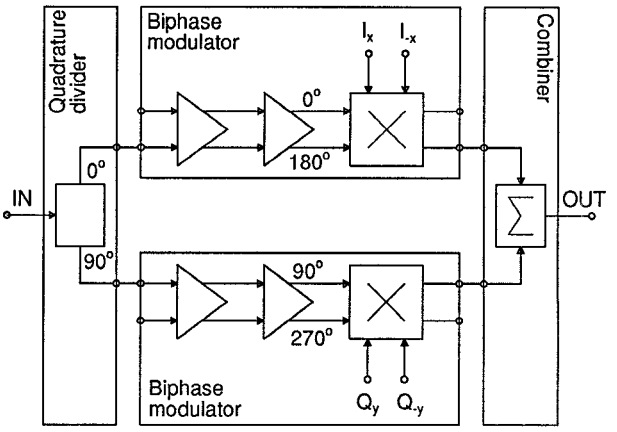

Figure 1: Simplified block diagram of the phase shifter.

Four orthogonal vectors are available at the outputs of the biphase modulators. The amplitude of each vector is independently controllable. Thus, supplying the control signals:

$$I_x + I_{-x} = A_x \cdot \cos(\theta) \qquad Q_y + Q_{-y} = A_y \cdot \sin(\theta)$$

will result in a vector with amplitude proportional to $\sqrt{\{A_x^2 + A_y^2\}}$ and an absolute insertion phase θ at the output of the combiner. Any desired vector between 0 and 360 degrees can thus be obtained.

MEASURED PERFORMANCE

The performance of the phase shifter MMICs are evaluated on wafer level. All circuits of five 2" wafers from 3 different batches are analyzed. An in-house test program cycles the phase shifter through all phase and amplitude states, controls an HP8510 network analyzer, additional equipment and the semi-automatic Alessi wafer prober. All measured S-parameters are recorded in a database. On-wafer measurements are made at room temperature.

The measured differential insertion phase of 128 phase states at maximum gain of a typical device across the frequency band from 6 to 12 GHz is shown in figure 2. The typical RMS phase error over the band from 7 to 10.5 GHz is 3 degrees, the RMS amplitude error is less than 0.3 dB.
The typical maximum obtainable gain over this band is 0 dB, input return loss is better than 15 dB and output return loss better than 10 dB.
The obtained improvement of this particular device with a correction for the systematic phase errors is shown in figure 3. The error correction is, in this case, performed with a look-up table.
Experiments indicated that the look-up table can be restricted to 32 frequency independent correction factors.
The RMS phase error distribution at 9 GHz over all wafers is plotted in figure 4. The RF yield of the devices that exhibit an uncorrected mean RMS phase error of about 3 degrees and a mean gain of 0 dB and good return losses is 50%.

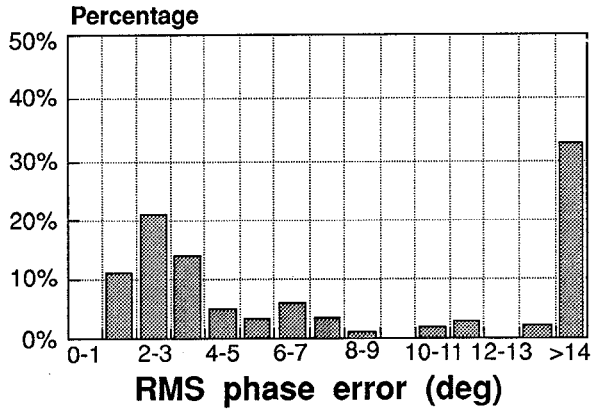

Figure 4: Statistical (uncorrected) RMS phase error distribution of all measured circuits.

The temperature performance of the vector modulator is analyzed in a fully operational transmit-receive module. The module was mounted on a temperature controllable Peltier element. Figure 5 shows the RMS phase temperature behaviour. The maximum worst-case hot-spot temperature within the circuit in CW operation is less than 75C at 55C of the Peltier element.

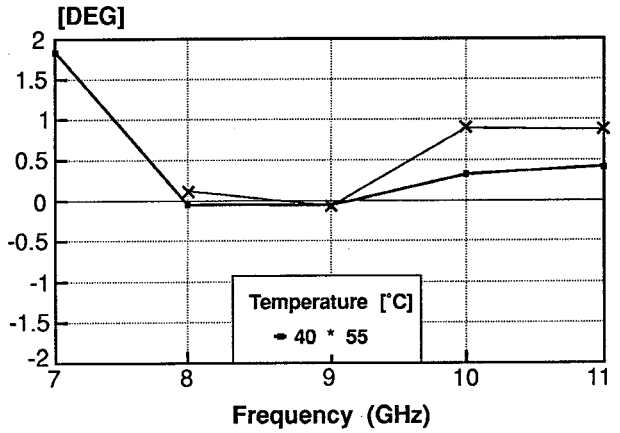

Figure 5: RMS phase error temperature behaviour. Reference temperature was 25C.

Finally, the typical overall performance at room temperature of the phase shifter is summarized in table 1. DC power consumption is less than 2 watts.

Frequency band	7.0 - 10.5 GHz
Gain	0 dB
Input return loss	> 15 dB
Output return loss	> 10 dB
Noise figure	10 dB
P_{1dB}	5 dBm
RMS phase error uncorrected	3.0°
RMS phase error corrected	< 0.7°
RMS amplitude error uncorrected	< 0.3 dB
RMS amplitude error with phase correction	< 0.3 dB
DC dissipation	< 2 watt

Table 1: Typical circuit performance.

MANUFACTURING AND CIRCUIT LAYOUT

The wafers are processed at the GaAs foundry of Philips Microwave Limeil with their standard D05ML process. This process includes 0.5 µm MESFETs, implanted GaAs resistors, NiCr resistors, MIM capacitors, spiral inductors, air bridges and via holes.

The chip size is 5.0 x 2.7 mm^2. A photograph is shown in figure 6. The FET count is 33. 25 Of them perform a RF function. Total gate width is 5.23 mm with FET sizes ranging from 80 µm to 450 µm. DC blocking and RF decoupling is fully done on chip. Total on-chip capacitance and via hole count is kept as low as possible in order to increase the DC yield. On-chip capacitance is less than 85 pF. Via hole count is 10. Great care is taken to avoid any RF feedback through the via holes. Only 3 DC supplies (7.5 volt, 5 volt and -5 volt) are needed to bias the circuit. On-chip resistive dividers and self-biasing techniques are used to bias the FETs.

A wide-band MMIC circuit operating at X-band with this complexity and level of integration is, to our knowledge, the first one to be demonstrated.

CONCLUSION

A single chip high performance phase shifter has been successfully developed. The device exhibits less than 3 degrees RMS phase error and less than 0.3 dB RMS amplitude error across a 30% bandwidth at X-band. Error correction reduces the RMS phase error to less than 0.7 degrees. Taking into account the complexity and size of the circuit, a high yield is obtained. The feasibility for phased-array applications is demonstrated.

ACKNOWLEDGMENT

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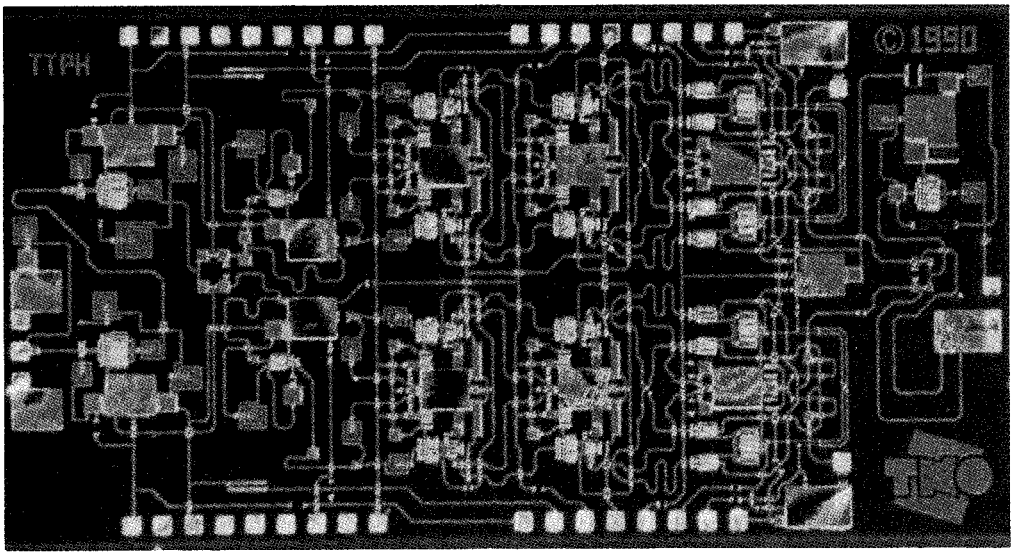
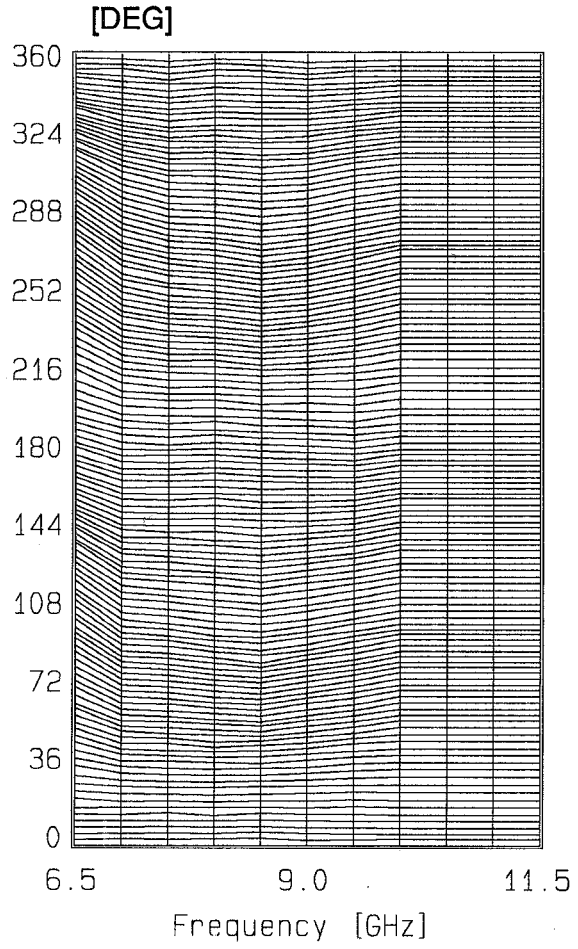


Figure 6: Photograph of the fabricated X-band phase shifter.



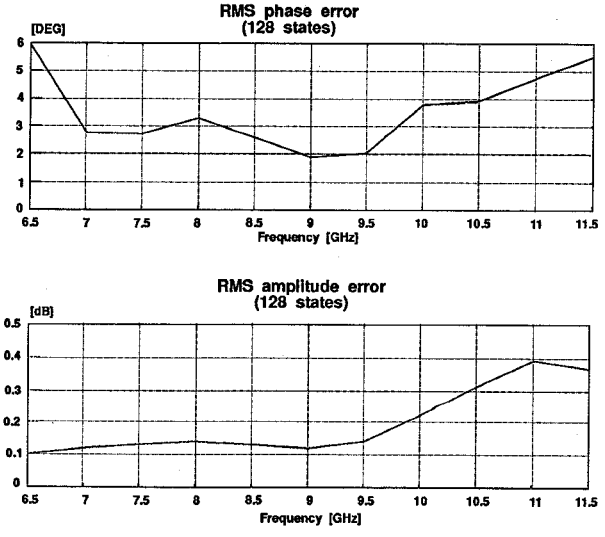
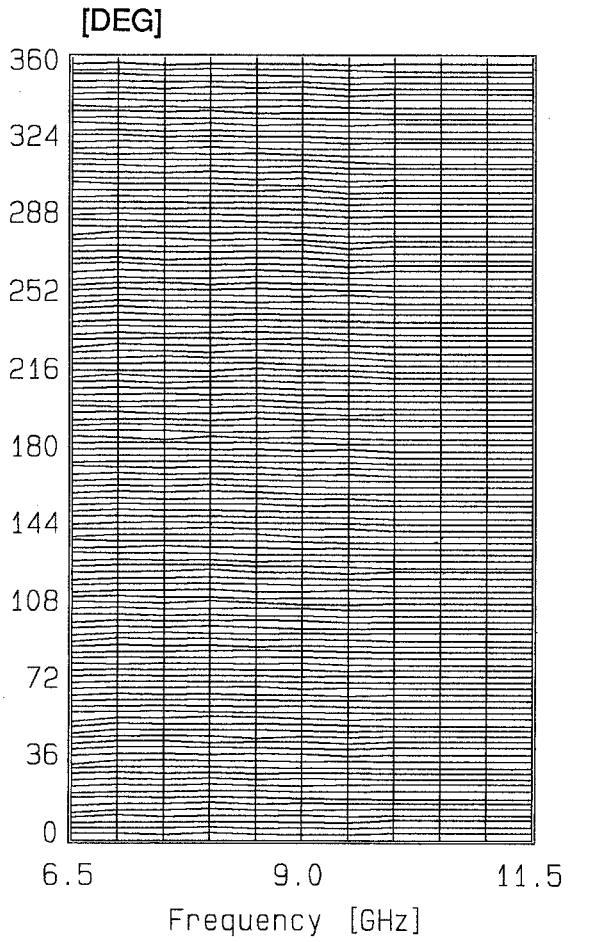


Figure 2: (top) Typical measured differential phase shift over 128 states with no error correction. (bottom) Associated RMS phase error and RMS amplitude error.



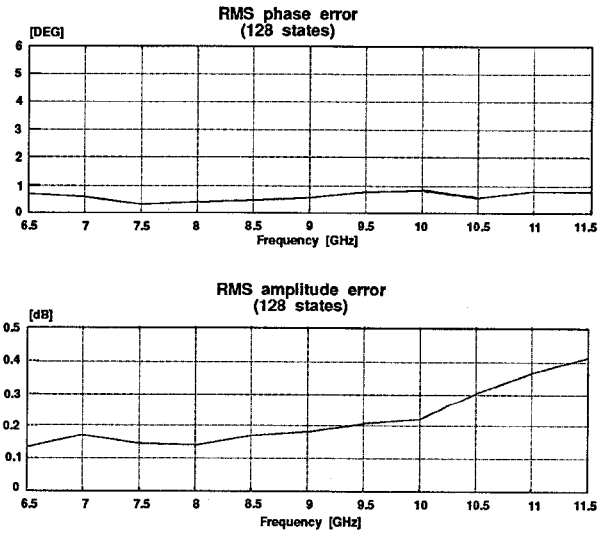


Figure 3: (top) Typical measured differential phase shift over 128 states with error correction. (bottom) Associated RMS phase error and RMS amplitude error.